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Title:

USING VECTOR NETWORK ANALYZER FOR ALIGNING OF TIME DOMAIN DATA

Inventor:

Timothy L. Hillstrom
23134 E. Settler Drive
Liberty Lake, WA 99019
Citizenship: US

USING VECTOR NETWORK ANALYZER FOR ALIGNING OF TIME DOMAIN DATA

TECHNICAL FIELD

[0001] The invention relates to electromagnetic devices and particularly to using a vector network analyzer for aligning of time domain data.

BACKGROUND OF THE INVENTION

[0002] Improving Voltage Standing-Wave Ratio (VSWR) is typically an iterative trial-and-error exercise when utilizing either frequency or time-domain information. For example, while circuit modifications which decrease Time Domain Reflectometry (TDR) "bumps" (discontinuities) are generally advantageous, decreasing a specific TDR bump does not necessarily improve VSWR within a frequency band of interest, but can actually degrade it.

BRIEF SUMMARY OF THE INVENTION

[0003] A method of using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement is provided. The method includes configuring the VNA for identifying discontinuities correlated to a VSWR lobe. In some embodiments, the method includes identifying a largest VSWR lobe in a frequency band of interest, using phase data associated with an S_{11} scattering parameter to find the correct electrical delay required to align Low Pass Step Transform data, and configuring the Low Pass Step Transform span and center time to align coherent inductive and capacitive discontinuities relative to grid lines of a TDR display. In some embodiments, the method is automated.

[0004] A system for concurrent frequency and time domain reflectometry measurements of an electromagnetic device is provided. The system includes a vector network analyzer (VNA) providing a visual display, and a processor associated with the VNA. The processor is operable to process the signal for graphic presentation on the visual display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIGURE 1 is a block diagram illustrating a typical TDR measurement system, in accordance with embodiments of the invention;

[0006] FIGURE 2 is a graph depicting a Low Pass Step Transform as a function of time on a TDR display;

[0007] FIGURE 3 is a flow diagram illustrating a measurement setup procedure (algorithm) for a VNA, in accordance with embodiments of the invention;

[0008] FIGURE 4 is a graph depicting a TDR display showing a Low Pass Step Transform measurement of a typical device under test (DUT), in accordance with embodiments of the invention;

[0009] FIGURE 5 is a graph illustrating the relationship between excess capacitance and discontinuity peak amplitude $|\rho_{pk}|$ specifically for an 18 GHz span and the NORMAL transform window of the Agilent Technologies PNA and 8510 VNAs, in accordance with embodiments of the invention;

[0010] FIGURE 6A is a flow diagram illustrating an iterative procedure, in accordance with embodiments of the invention; and

[0011] FIGURE 6B is a flow diagram illustrating automated implementation of the measurement setup procedure of FIGURE 3, in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0012] By using both frequency and time domain reflection measurements in conjunction, it is possible to positively identify the specific circuit discontinuities which contribute to a given Voltage Standing-Wave Ratio (VSWR) lobe. Optionally, corrective action can then be readily determined for optimum VSWR performance. VSWR is a well-known measure of reflections from a device.

[0013] Improving VSWR is typically an iterative trial-and-error exercise when utilizing either frequency or time-domain information. For example, while circuit

modifications which decrease Time Domain Reflectometry (TDR) "bumps" (discontinuities) are generally advantageous, decreasing a specific TDR bump does not necessarily improve VSWR within a frequency band of interest, but can actually degrade it.

[0014] However, by using information in both frequency and time domains concurrently, one can determine specific TDR discontinuities which contribute to specific VSWR lobes. This is performed advantageously using a Vector Network Analyzer (VNA), which measures time domain reflection data from a device, because: (1) vector data is necessary to transform to a TDR display; and (2) phase information in the S_{11} data is necessary to find the correct time alignment of the TDR data. S_{11} is a vector "scattering parameter," which measures the fractional reflected signal from a device. It is directly related to VSWR, as described below in more detail. S_{11} and VSWR are both frequency-domain parameters. Lobes are local peaks, which look like randomized peaks located along the x-axis in an S_{11} or VSWR measurement display. The lobes denote local maxima of reflected energy, which degrade the performance of a device.

[0015] FIGURE 1 is a block diagram illustrating typical TDR measurement system 100, in accordance with embodiments of the invention. VNA 11 interfaces with DUT 15 through a standard coax cable 18 and RF connector 19 (usually type-N or SMA). Processor 16 associated with VNA 11 converts the measurement signal data into TDR display 12. In alternative embodiments, circuitry internal to VNA 11 performs the functions of processor 16. VNA 11 provides a user interface, for example control panel 14, and user-scrollable display marker 17 having a dot, triangle, or other recognizable shape.

[0016] Although the terms VSWR and S_{11} are in practice often used interchangeably, S_{11} specifically contains the necessary phase information. VSWR and S_{11} are alternative representations of reflected energy related to one another by Equation (1):

$$VSWR = (1 + |S_{11}|)/(1 - |S_{11}|) \quad (1)$$

[0017] Although scaled differently, both quantities increase with increasing reflected energy.

[0018] There are multiple versions of TDR measurements and transforms. A useful version for purposes of illustration is a "Low Pass Step Transform." This is a menu

choice on commercially available VNAs, for example the Agilent Technology PNA (acronym for "performance network analyzer") and 8510 Vector Network Analyzers. More detailed information regarding these instruments may be found in their respective product data sheets available at the Agilent Technologies web page on the Internet, http: / we.home.agilent.com/.

[0019] FIGURE 2 is a graph depicting Low Pass Step Transform 201 as a function of time using an arbitrary scale on TDR display 12. Time scales are typically in a range from tenths of a nanosecond per division to a few nanoseconds per division. As shown in FIGURE 2, the Low Pass Step Transform is advantageous, because it clearly identifies capacitive, inductive, and resistive discontinuities. The term "capacitive discontinuity" refers implicitly to a region of excess shunt capacitance on the TDR display, whereas "inductive discontinuity" refers implicitly to a region of excess series inductance on the TDR display. Excess capacitance or excess inductance is typically localized to a small physical region in a circuit under test.

[0020] Mathematically, the Low Pass Step Transform is the integral of the Inverse Fourier Transform of the windowed vector- S_{11}. This transform mathematically relates TDR discontinuities to VSWR lobes. The broadly used term "windowed" refers to a specific weighting function applied to the pre-transform data. Windowing is required to prevent "leakage" after the Transform process. A window is a standard feature on many instruments, including all Agilent Technologies Digital Signal Processing (DSP) instruments.

[0021] As depicted in FIGURE 2, a single small capacitive discontinuity of a TDR at $t = 0$ generates a negative bump 210 in Low Pass Step Transform 201. If other capacitive bumps are added at times $t = M * \tau$, where M is an integer and τ is any arbitrary time interval, VSWR lobes are created at frequencies $f = N/\tau$, where N is an independent integer. This is because the phase at $f = N/\tau$ due to each capacitive bump is the same, so that energy addition is coherent and maximized. This is most easily understood as delay between capacitive bumps being an integer number of periods at frequency $f = N/\tau$. Similarly, if inductive discontinuities, for example bump 202 (positive in Low Pass Step Transform 201) are added at times $t = (M + 0.5) * \tau$, they will also add coherently to the VSWR lobe at frequency $f = 1/\tau$ and its odd harmonics. There is no relationship between M

and N, which simply denote periodicity in the respective time and frequency domains. Consequently, the combination of their inverted time amplitude (relative to capacitive bumps 210) and their half-cycle delay results in S_{11} phase equal to that due to capacitive bump 210, such that they constructively add.

[0022] In practice, a TDR measurement reveals a variety of discontinuities of varying size, spacing, and type (capacitive, inductive, or resistive). FIGURE 2 for example depicts both abrupt 203 and gradual 204 resistive discontinuities. Nonetheless, the S_{11} lobes represent those frequencies where the energy is most constructive (i.e., coherent), and the VSWR local minima are those frequencies where the energy is most canceled. By properly specifying the TDR measurement, based on information from the S_{11} measurement, those TDR discontinuities which are coherent for a given VSWR lobe, as well as those which are canceling and orthogonal, can be unambiguously identified. Embodiments of the invention provide the following general capabilities:

(1) Use of a broadband Vector Network Analyzer for coordinated VSWR and TDR measurement.

(2) Configuration for identifying discontinuities correlated to a VSWR lobe.

(3) Calibrating the capacitive, inductive, and resistive discontinuities.

[0023] Frequency-domain measurements of VSWR or S_{11} typically show a series of lobes. As described above, these are predominantly caused by phasing, due to the combination of size, type, and delay of the set of time-domain discontinuities. One or more lobes may occur in the frequency band where a design requires the lowest VSWR. Optimally, tuning efforts are focused on those circuit elements that contribute coherently to problem lobe(s). FIGURE 3 is a flow diagram illustrating measurement setup procedure (algorithm) 300 for a VNA, in accordance with an embodiment of the invention, which includes the following operations:

(1) Ensure a valid 1-port calibration has been performed on the VNA, as depicted in operation 302. This calibration is performed at a defined physical plane at RF connector 19;

(2) Set Channel 1 to Low Pass Step Transform, and Channel 2 to S_{11}, as depicted in operation 303;

(3) Find f_0, the frequency at the peak amplitude of the largest S_{11} lobe in the frequency band of interest, as depicted in operation 304;

(4) Set Electrical Delay to zero, then find the phase of S_{11} at f_0, and denote this phase θ (degrees), as depicted in operation 305;

(5) Set Electrical Delay in both channels to $(90-\theta)/(360*f_0)$, as depicted in operation 306;

(6) Check phase (S_{11} lobe) equal zero degrees, as depicted in operation 307; and

(7) Set Channel 1 Span to $10/f_0$; Center to 0.4*span; Format to Real; Ref Position to 5 Divisions; Ref Value to zero; and Scale to 0.05 Units/division, as depicted in operation 308.

[0024] Measurement setup procedure 300 provides a powerful visual tool in emphasizing circuit modifications on those circuit discontinuities which directly (coherently) contribute to a problem VSWR lobe. By observing the TDR and S_{11} displays concurrently, the relationships of discontinuity location and type to S_{11} lobe magnitude follow a set of rules.

[0025] FIGURE 4 is a graph depicting TDR display 12 showing a Low Pass Step Transform measurement 401 of a typical device under test, in accordance with embodiments of the invention. FIGURE 4 shows an example of TDR display 12 for the case in which a problem VSWR lobe is located at 2.2388 GHz. The x-axis scaling is specified in accordance with setup procedure 300, such that the scale is $1/f_0$ per division, which corresponds to a total time span of $10/f_0$ for displays with 10 x-axis divisions. For example, if f_0=2 GHz, then the x-axis scale should be 0.5 nanosecond per division, or a total time span of 5 nanoseconds.

[0026] FIGURE 4 depicts examples of coherent, orthogonal, and canceling discontinuities. Using setup procedure 300, all coherent discontinuities 402a-402c are positive (inductive) aligned with x-axis gridlines, for example 411-413, or are negative 403-405 (capacitive) aligned at midpoints between consecutive x-axis gridlines. Discontinuities at 25 per cent 406a or 75 per cent 406b, 407 within an x-axis division are orthogonal to the lobe energy and therefore make very low reflective contribution. In fact, the orthogonal energy across the entire TDR must sum to zero at the lobe frequency, since the transformed phase is exactly 90 degrees (after Electrical Delay adjustment) for the Low Pass Step Transform. These relationships can typically be verified by moving a small capacitive probe along the electrical path of the circuit under test.

[0027] Equally important, any capacitive bumps on vertical x-axis gridlines, for example discontinuity 409, actually cancel energy at the lobe of interest and therefore require no correction. This is also true for any inductive bumps, for example inductive discontinuity 408, at the midpoints between consecutive x-axis gridlines.

[0028] The reason why the 90 degree condition rather than the zero degree condition is used for time alignment is that the Low Pass Step Transform is the time integral of the Low Pass Impulse response, which is the direct Fourier transform of broadband S_{11} scattering parameter. The time integral corresponds to a 90 degree phase shift in S_{11}. The time integral mathematical representation is also consistent with the observed magnitude increase of successive VSWR lobes with frequency. The time derivative in the inverse transform definition generates a $2\pi * f$ multiplier in S_{11}.

[0029] For the purpose of designing circuit modifications to correct or compensate identified TDR discontinuities of interest, it is important to know the magnitude of excess capacitance, inductance, or resistance causing the discontinuity. For calibration of resistance discontinuities, the resistance (or impedance) change is,

$$\Delta R = Z_0 * (1 + \rho_{\tau+})/(1 - \rho_{\tau+}) - Z_0 * (1 + \rho_{\tau-})/(1 - \rho_{\tau-}) \quad (2)$$

where $\rho_{\tau-}$ is the TDR amplitude immediately before the resistive discontinuity, and $\rho_{\tau+}$ is the TDR amplitude immediately after the resistive discontinuity.

[0030] For small resistive discontinuities,

$$\Delta R =\sim 2 * Z_0 * \Delta\rho \quad \text{for } \Delta\rho < 0.1 \tag{3}$$

[0031] For capacitive discontinuities, the Low Pass Step Transform in an infinite bandwidth system is:

$$\rho(t) = -u(t) * e^{-2t/(C*Z0)} \tag{4}$$

[0032] The parameter ρ(t) in Equation (4) represents time-domain reflection as a function of time, as shown in examples in FIGURES 2 and 4, where *u(t)* represents the unit step function. With infinite bandwidth, each capacitive or inductive bump would be described by Equation (4) (and delayed in time by some amount). However, band-limited measurement causes the unit-exponentials to be spread in time and reduced in amplitude, with the resulting appearance in FIGURES 2 and 4.

[0033] For $C = 0.1\,\text{pF}$ and $Z_0 = 50\Omega$, the time constant of this exponential pulse is 2.5 picoseconds with a corresponding bandwidth of about 64 GHz. Therefore, an 18 GHz VNA will limit the bandwidth of the pulse, lowering the amplitude and spreading it. Furthermore, the S_{11} information is windowed prior to transform to prevent ringing in the TDR, reducing the TDR bandwidth to roughly 7 GHz, depending on the window chosen in the Transform setup. The displayed capacitive discontinuity is the time convolution of the VNA transform impulse response with the ideal response of Equation (4). In FIGURE 4, label 0.0 identifies the y-axis reference value of 0.0 units.

[0034] FIGURE 5 is a graph illustrating the relationship between excess capacitance versus discontinuity peak amplitude $|\rho_{pk}|$, in accordance with embodiments of the invention. The relationship in FIGURE 5 specifically applies to an 18 GHz span and the NORMAL transform window of the Agilent Technologies PNA and 8510 VNAs, which use Kaiser-Bessel windowing. Curve 502 shows the analytical relationship between excess capacitance versus $|\rho_{pk}|$, whereas straight line 501 shows a linear approximation of the relationship, in accordance with Equation (5) below:

$$C =\sim Kc * \left|\rho_{pk}\right| \qquad \text{for } \left|\rho_{pk}\right| < 0.1\ , \tag{5}$$

[0035] where the constant of proportionality for capacitance is

$$Kc = 1.9\text{pF}.$$

[0036] The parameter $|\rho_{pk}|$ in Equation (5) is the peak amplitude of an isolated capacitive or inductive "bump" in the $\rho(t)$ trace, for example 202, 210, 402a-402c, and 408. The $|\rho_{pk}|$ of a specific capacitive bump is directly related to the amount of "excess capacitance. " The relationship is calculated in Equation (5) and displayed in curve 502 of FIGURE 5. For small bumps ($|\rho_{pk}|<0.1$) the relationship is approximately linear, as shown in line 501 of FIGURE 5. If, for example, the scale of FIGURE 2 is 0.05 units per division, then for capacitive "bump" 210, $|\rho_{pk}| = 0.06$ (approximately). The value is measured from the "base" of the bump to the peak.

[0037] For small capacitive discontinuities (i.e. <0.2 pF), the peak amplitude $|\rho_{pk}|$ of the measured capacitive bump is approximately proportional to the excess capacitance. With specific knowledge of the frequency-domain windowing, this relationship can be derived analytically, but in practice it is simple to calibrate it physically using a conventional tuning stub of known capacitance.

[0038] Inductive discontinuities behave similarly to capacitive discontinuities, but with positive amplitude. Once the proportionality constant for capacitance has been determined as in Equation (5), the proportionality constant for inductance can be calculated as,

$$K_L = Z_0^2 * Kc, \tag{6}$$

[0039] And the relationship for excess inductance is similarly,

$$L =\sim K_L * \left|\rho_{pk}\right| \qquad \text{for } \left|\rho_{pk}\right| < 0.1 \tag{7}$$

where, in this case, $K_L = 4.75\text{nH}$.

[0040] A deterministic method of VSWR optimization has been described. The method requires a broadband VNA with Time Domain transform capability, for example the Agilent Technologies PNA and 8510 VNAs, for concurrent measurements of S_{11} scattering

parameter and Low Pass Step Transform. FIGURE 6A is a flow diagram illustrating iterative procedure 610, including the following method operations:

1) In operation 612, the user identifies the largest VSWR lobe in the frequency band of interest; and uses S_{11} phase data to find the correct electrical delay required to align the Low Pass Step Transform data.

2) In operation 613, the user configures the Low Pass Step Transform span and center time to place coherent inductive discontinuities on grid lines, and coherent capacitive discontinuities at grid midpoints.

3) In operation 614, the user identifies the problem discontinuities. Calibration of the discontinuity magnitude allows the design of correctly sized compensating features.

4) In operation 615, the user repeats the procedure for any other problem VSWR lobes in the frequency band of interest, in order of decreasing lobe magnitude.

[0041] Operations 612, 613, and 615 will be recognized as essentially similar to the operations depicted in procedure 300 of FIGURE 3, whereas operation 614 depicts the calibration operation described in connection with FIGURE 5. This method eliminates a substantial majority of trial-and-error iteration required by methods relying solely or serially on time domain or frequency domain measurement. It is the concurrent methodology and measurement capability which enables positive determination of those circuit discontinuities which coherently contribute to any given VSWR lobe.

[0042] The above paragraphs describe only a manual implementation of TDR for analysis of circuit discontinuities and VSWR lobes. The manual method can be time-consuming, repetitive, and error-prone due to the multiple steps. Advantageously, a VNA, for example the Agilent PNA or 8510, can automatically implement these steps, thereby saving user time and reducing errors. FIGURE 6B is a flow diagram illustrating automated implementation of the operations of the measurement setup procedure of FIGURE 3, in accordance with embodiments of the invention.

(1) User provides a suitable VNA in operation 602. Then in operation 603, the user places a marker on a VSWR or S_{11} lobe of interest. A marker is a conventional dot or other symbol, for example the triangular marker shown in FIGURE 1, that is user-scrollable across a display trace. The x-axis and y-axis coordinates are displayed for the current marker position.

(2) In operation 604, the user presses a control key labeled, for example, "Coherent Time," thereby initiating automated execution of the procedure described in connection with FIGURE 3;

(3) In operation 605, the Vector Network Analyzer automatically performs steps described above in connection with setup procedure 300 of FIGURE 3;

(4) In operation 606, a Low Pass Step Transform is displayed with correct time alignment for identifying coherent, canceling, and orthogonal circuit discontinuities.

[0043] The automatic implementation requires: (1) A VNA having marker and internal processor capable of VNA state control and vector math; and (2) An algorithm which generates the desired display of "coherent, canceling, and orthogonal discontinuities."

[0044] Optionally, operation 614 of FIGURE 6A can also be automated, providing automatic calibration of excess capacitance and excess inductance versus TDR discontinuity magnitude. This can, for example, be performed using a special marker or providing on the display the coefficients of proportionality.

[0045] While the invention has been described in conjunction with specific embodiments, it is evident to those skilled in the art that many alternatives, modifications, and variations will be apparent in light of the foregoing description. Accordingly, the invention is intended to embrace all other such alternatives, modifications, and variations that fall within the spirit and scope of the appended claims.